The Effect of Nano-Ribbon Thickness on the Graphane Filed Effect Transistor

Majid Heidari, Rahim Ghayour, Masoud Mahzoon

***Abstract*— this article studied the effect of thickness on the characteristic Graphene field of transistor. Transistors Graphene have been developed quickly. So, it consider as a choice of electronic after silicon.**

It shows that if the thickness of Graphene to be increase , the flow drain to be increase, so, we have more negative voltage and also it cause that energy Graphene to become zero , finally drain current is not saturated.

***Index Terms*— Field effect transistor, Graphane, Nano-ribbon, Thickness.**

I. Introduction

Just now, transistors Graphene have been developed quickly, so it consider as a choice of electronic after silicon. Nevertheless most of details about performance of Graphene transistor in actual use are unknown.

Against of predictions, main characteristic of Graphene is not high mobility Transistor. For developed Graphene on oxide silicon mobility is considered as 4000 cm-2 u-1.s-1 in normal temperature insect. Making transistor whit narrow channel & without side effect is considerable.

For large width of Graphene the energy gap is zone so, because of it transistors made of Graphene can't be turn off and are not useful for switching but we can modify this graph into three method: limiting large width of graph to one aspect it means using Nano-ribbon with force low pressure & tension on the graph structure or implementation extern field on bilayer of graph.

By using methods energy gap could be create 200-250 MEV. However the number of made transistor is increasing but also dominant challenges of graph transistor consist of creating suitable energy gap. Creating large width with correct performance in zone of saturation is difference but also most of researches had been done on the field effect transistor, Are three shapes: first structure only conclude low gate. So, because of having big parasite capacitor has considered as an impractical structure.

According to the done researches practical Graphene transistor need to structures that gate has install on channel.

This structure make in two shapes: In the first structure one layer of silicon to be grow under the substrate then grow Graphene on it until channels of graph to be making. In the second structure, the layer of carbide silicon is choosing and on which a layer of gape as a channel grow.

Manuscript received November 24, 2015.

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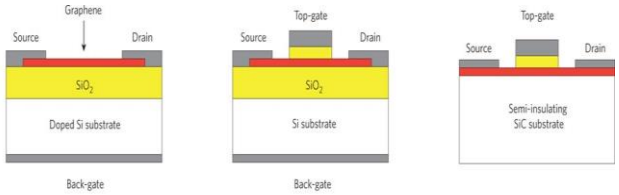

Fig (1): Filed effect transistor made structures consist of graph (GFET).

In this article we select the second structure, Whit stimulation it by using software SILVACO TCAD. At first, study steps of making on the environment Athena as like as process make then analysis transistor environment Athena to extract characteristic of transistor.

Like threshold voltage and drain current. The process of making GFET to be stood by growing under the substrate with length of 1.2 µm and high 1 µm. Consist of trivalent element bore P-type impurity to be create on it. Then during the process 300 mm silicon change into Oxide silicon. So because of it we don't identify Graphene in software SILVACO therefore we used of substitute material.

We identify characteristic of Graphene like energy gap capability of motion electron, ext. during the process. As a reason, we identify one layer of poly silicon with 5 mm thickness. Consist of impure element arsenic on Oxide silicon as a channel. Then identify one layer of oxide silicon whit 1 mm thickness on the poly silicon as an oxide gate.

We used drain source of aluminum for creating gate terminal and finally transistor structure to b complete. By filling the blank of terminals for source and drain by gate, made structure to be saved in envierment Athena then to be used for analysis transistor parameters. Two – dimensional GFET structure has been shown in figure (2).

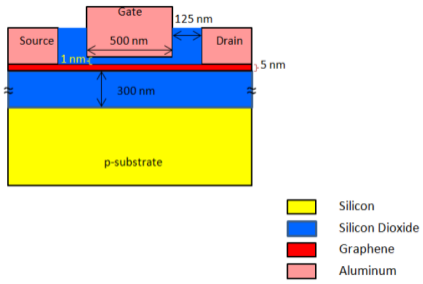

Fig (2): Two – dimensional GFET structure

Presented structure consist of length of 1.2 µm substrate height 0.65. So as a layer of silicon oxide by thickness of 300 mm set on it. Then a layer of Graphene by thickness of 5 nm as a channel put on it. So because of high gravity for carrier aluminum metal use as a connector drain & source to be directly connect to channel. In other hand parts of Graphene

channel below the gate connector act as a drain & source regions In above the channel on thin layer put as a gate oxide then one metal with length of 500 mm lay on it. Table (1) show effect of width ribbon on transistor characteristics.

Table (1): effect of width ribbon on transistor characteristics

Thickness	1 nm	5 nm	10 nm	30 nm
V_{th}	-0.833 V	-2.74 V	-4.8 V	-6.9 V
I_D	0.48 mA	2.13 mA	3.95 mA	10 mA
F_T	3.25 GHz	6.5 GHz	12.26 GHz	7.8 GHz
F_{MAX}	6.01 GHz	10.2 GHz	23.6 GHz	12.6 GHz

II. Stimulation

By observing results we can understand that the increasing thickness of part Graphene lead to increasing drain current so, we have more negative voltage.

As we told, this thickness cause that energy gap to become zero, finally drain current isn't saturated. This subject is completely clear in curve ID-UDS With width 30 nm but we observe decreasing for more 10 nm width.

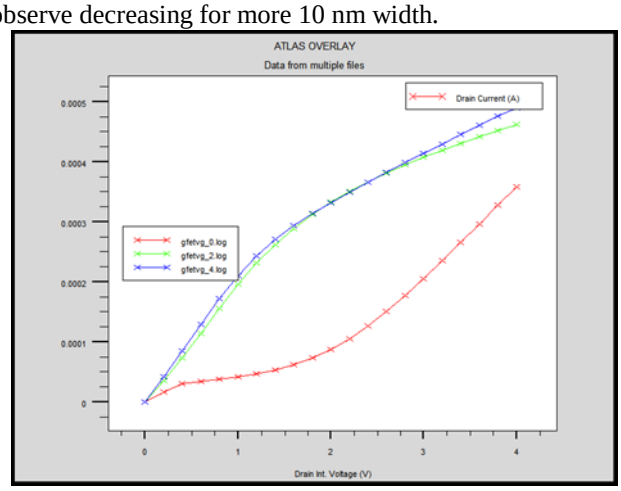

Fig (3): I_d-V_{ds} Curve for 1 nm width

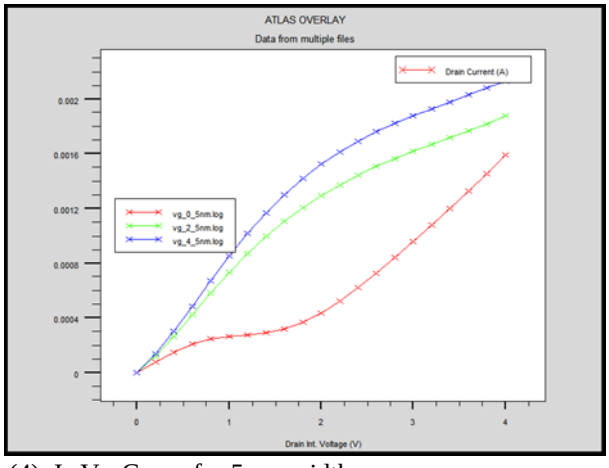

Fig (4): I_d-V_{ds} Curve for 5 nm width

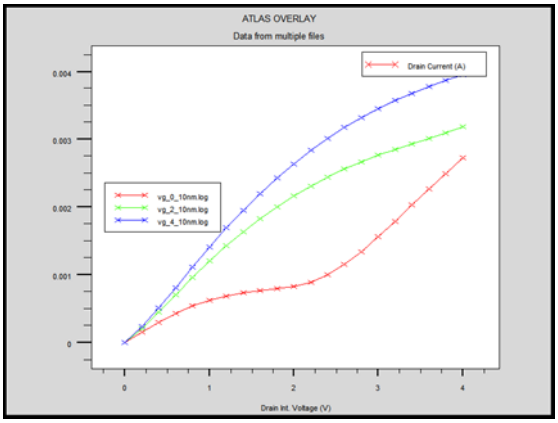

Fig (5): I_d-V_{ds} Curve for 10 nm width

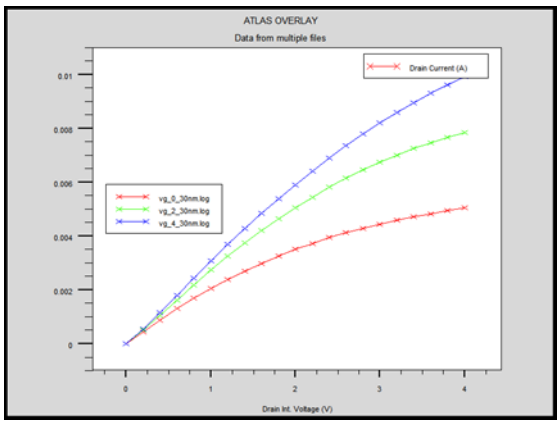

Fig (5): I_d-V_{ds} Curve for 30 nm width

III. Conclusion

This article studied on the effect of thickness Graphene on the characteristic of transistor on the Graphene field.It shows that if the thickness of Graphene to be increase, the flow drain to be increase .so, we have more negative voltage and also in cause that energy gap to become zero, finally drain current isn't saturated.

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