Hybrid Technique Based VLSI Design Automation

Kiranpreet Singh, Sandeep Singh, Ramandeep Singh

***Abstract*— The efficient designing of any complex system necessitates decomposition of the same into a set of smaller subsystems and each subsystem can be designed independently to speed up the design process. Partitioning is one of the fundamental problems of VLSI physical design. The aim of present study is to do the Bi partitioning of the VLSI circuit using Hybrid Algorithm. The combination of Simulated annealing and Genetic Algorithm is used to improve the speed while using moderate storage Hybrid Algorithm (HA) is expected to provide better solution with less CPU time. Based on the results of study, the hybrid algorithm is shown to produce promising results when applied to circuit partitioning problem. The algorithm not only balances the size of two portions but also evenly distributes the connections among them. Parent selection strategy employed avoids the premature convergence of HA to a local optimum.**

***Index Terms*— Hyper graph partitioning algorithm, FPGA, Multi-pin net model, Multi hyper graph partitioning algorithm.**

I. INTRODUCTION

The efficient designing of any complex system necessitates decomposition of the same into a set of smaller subsystems. Subsequently, each subsystem can be designed independently to speed up the design process. Partitioning is used in various EDA applications, e.g., as a tool for placement algorithm or for assigning circuit elements to blocks that can be packaged separately. In VLSI design applications, Partitioning are used to achieve various objectives such as Circuit Simulation, Circuit Layout and Circuit Packaging **(Mazumder and Rudnick, 2003).**

The Partitioning of a system into a group of PCBs is called System level partitioning. The Partitioning of a PCB into chips is called Board level partitioning while partitioning of a chip into smaller sub circuits called Chip level partitioning. At each level, constraints and objectives of the partitioning process are different as discussed below **(Seche and Chen, 1988).** The circuit assigned to a PCB must satisfy certain constraints. Each PCB has a fixed area, and fixed number of terminals to connect with other boards. The number of terminals available in one board to connect to other boards is called the terminal count of the board.

The board level partitioning faces a different set of constraints and fulfills a different of objectives as a opposed to system level partitioning. Unlike boards chips can have different sizes and can accommodate different no. of terminals. Typically the dimension of chip range from 2mm* 2mm to 25mm*25mm.While system level partitioning is geared towards satisfying the area and the terminal constraints of each partition, board level partitioning ventures to minimize the area of each chip. Minimize the number of chip is another important determinant of performance because the off chip delay is much larger than the on chip delay. The Partitioning problem at any level or design style deals with one or more of the following parameters **(Wolf, 2004).**

1. Interconnections between Partitions: The numbers of interconnections at any level of partitioning have to be minimized. Reducing the interconnections not only reduces the delay but also reduces the interface between the partitions making it easier for independent design and fabrication.

2. Delay due to the Partitioning: The partitioning of a circuit might cause a critical path to go in between partition a number of times. As the delay between partitions is significantly larger than the delay with in partition, this is an important factor which has to be considered while partitioning high performance circuits.

3. Number of Terminals: Partitioning algorithms at any level must partition the circuit so that the no. of nets required to connect a sub circuit to other sub circuits does not exceed the terminal count of the sub circuit. In case of system level partitioning. Partitioning algorithms (Donald, 2004) can be classified in different ways.

There are two classes of partitioning algorithm under this classification scheme:

Constructive algorithm: The input to a constructive algorithm is the circuit components and the net list. The output is set of partition and the new net list. These algorithms are typically used to form some initial partitions which can be improved by using other algorithm.

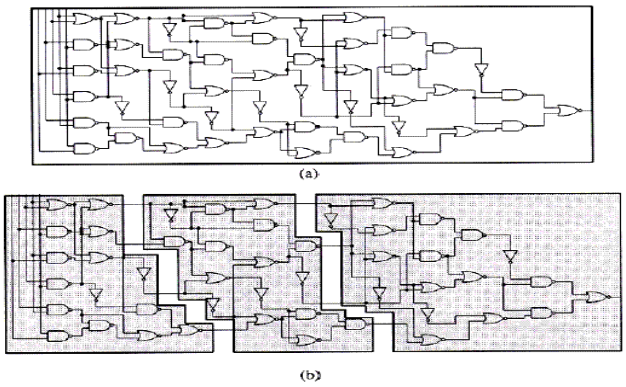

Fig. 1 Partitioning of a circuit

Iterative algorithm: These algorithms accept a set of partitions and the net list as input and generate an improved set of partitions with the modified net list. These algorithm

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Kiranpreet Singh, Department of Electronics and Communication Engineering, Guru Nanak Dev Engineering College, Ludhiana, 141002, India

Sandeep Singh, Department of Electronics and Communication Engineering, Guru Nanak Dev Engineering College, Ludhiana, 141002, India

Ramandeep Singh, Department of Electronics and Communication Engineering, Guru Nanak Dev Engineering College, Ludhiana, 141002, India

iterate continuously until the partitions cannot be improved further.

Evolution based algorithm belongs to the probability and iterative class of algorithm for combinatorial optimization problems (Dahiya et.al., 2007). Static problems are those in which the characteristics of the problem are given once and for all when the problem is defined and don't changes while the problem are solved. On the contrary, dynamic problems are defined as a function of some quantities whose value is set by the dynamics of an underlying system (Dorigo and Stutzel, 2005).

II. PROBLEM FORMULATION

The partitioning problem can be expressed more naturally in graph theoretic terms. A Hyper graph G = (V,E) representing a partitioning problem can be constructed as follows. Let V = $\{v_1, v_2, \ldots\ldots\ldots, v_n\}$be a set of vertices and E = $\{e_1, e_2, \ldots, e_m\}$ be a set of hyperedges. Each vertex represents a component. There is a hyper edge joining the vertices whenever the components corresponding to these vertices are to be connected. Thus, each hyper edge is a subset of the vertex set i.e., $e_i \subseteq V$, i = 1, 2,…., m. In other words, each net is represented by a hyper edge. The area of each component is denoted as a (vi), $1 \leq i \leq n$. The modeling of partitioning problem into hyper graphs allows us to represent the circuit partitioning problem completely as a hyper graph partitioning problem .Partition is also referred to as a cut. The cost of partition is called the cut size, which is the number of hyper edges crossing the cut.

A. *OBJECTIVE*

Partitioning is one of the fundamental problems of VLSI physical design. **Our aim is to do the Bi partitioning of the VLSI circuit using Hybrid Algorithm**. The simplest partitioning problem is a partition on the two subsets (two way partitioning problem) which can be formulated as a graph partitioning problem.

B. *Hybrid Algorithm for circuit partitioning*

HA is a search technique for global optimization in a complex search space. Search space in HA is composed of possible solutions to the problem. A solution in the search space is represented by a sequence of 0s and 1s. This solution string is referred to as the chromosome in the search space. Each chromosome has an associated objective value called the fitness value. The fitness of a chromosome corresponds to its ability to survive and reproduce offspring. A good chromosome (that has good chance to survive) is the one that has a high/low fitness value depending upon the problem (maximization/ minimization). A set of chromosomes and associated fitness values are called the population. This population at a given stage of the GA is referred to as generation.

In this work, I have implemented hybrid algorithm in Matlab 7.5 to solve circuit bi partitioning problem. The circuit partitioning problem can be considered **as** a generalized version of the well known graph partitioning problem. Hence, several graph partitioning algorithms have been used with or without modifications for solving this problem. The graph partitioning problem is known to be NP-complete and several heuristic algorithms have been proposed in past. Hybrid algorithm combines SA and GA to improve the performance.

C. *Methodology:*

The proposed method is divided into following steps:-

Step1: Procedure starts by inputting circuit of desired nodes from the net list having 10 to 199 nodes. Each benchmark comes with 3 files, a .net file, a .are file and a .netD file. Following is the format of net list. The list of nets follows. Each net is simply a subset of modules which are either cells or pads. Cells are numbered from 0 to pad offset (inclusive). Pads are numbered from 1 to (#Modules - pad offset - 1).Cells are prefaced by an "a", pads by a "p".

III. . RESULTS AND DISCUSSION

Circuit Bi-partitioning belongs to a class of non-deterministic polynomial complete (NP-complete) which has multiple answers. In our work we have solved this problem using Hybrid algorithm which is implemented in MATLAB version 7.5. HA improves speed using moderate storage as compared to most commonly used optimization schemes for circuit portioning.

Table 1. Effect of variation in threshold on Min cut

S. No.	Circuit	No. of nodes	Temp. Cooling Rate	Threshold	Min cut
1	spp_N100_E103_R6_332.netD	102	400, 0.5	170	16
2	spp_N100_E103_R6_332.netD	102	400, 0.5	190	13
3	spp_N100_E103_R6_332.netD	102	400, 0.5	210	20
4	spp_N100_E103_R6_332.netD	102	400, 0.5	230	20
5	spp_N100_E103_R6_332.netD	102	400, 0.5	250	20
6	spp_N100_E103_R6_332.netD	102	400, 0.5	270	19
7	spp_N100_E103_R6_332.netD	102	400, 0.5	290	19
8	spp_N100_E103_R6_332.netD	102	400, 250	310	19
9	spp_N100_E103_R6_332.netD	102	400, 250	330	17

Table 5.2: Effect of variation in threshold on Min cut

S. No.	Circuit	No. of nodes	Temp. Cooling Rate	Threshold	Min cut
1	spp_N100_E103_R6_332.netD	102	400, 0.5	170	16
2	spp_N100_E103_R6_332.netD	102	400, 0.5	190	13
3	spp_N100_E103_R6_332.netD	102	400, 0.5	210	20
4	spp_N100_E103_R6_332.netD	102	400, 0.5	230	20
5	spp_N100_E103_R6_332.netD	102	400, 0.5	250	20
6	spp_N100_E103_R6_332.netD	102	400, 0.5	270	19
7	spp_N100_E103_R6_332.netD	102	400, 0.5	290	19
8	spp_N100_E103_R6_332.netD	102	400, 250	310	19
9	spp_N100_E103_R6_332.netD	102	400, 250	330	17

During experimentation we change all the parameters of HA. As one of the parameters changes its value the others are fixed in order to determine influence on the parameter in the focus. If we ignore the swing value, the best results are obtained for population size=20, initial temperature T_o = 400, cooling rate α = 0.5,threshold=190.

IV. CONCLUSIONS

A new algorithm has been presented to improve the performance and use less resource in circuit partitioning which is a very important step in the back-end design flow. The new algorithm, Hybrid Algorithm (HA), is the combination between Simulated Annealing Algorithm (SA) and Genetic Algorithm (GA). Based on the results of study, the hybrid algorithm is shown to produce promising results when applied to circuit partitioning problem. The algorithm not only balances the size of two portions but also evenly distributes the connections among them. Parent selection strategy employed avoids the premature convergence of HA to a local optimum. Mutation process permits population diversity to be maintained. Various parameters affecting the algorithm are studied and their influence on convergence to final optimal solution is shown. With proper selection of parameters of HA minimum value of min cut can be obtained.

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