Low Noise Wireless Modem for Patient ECG Signal Transfer Based SDR Technology and FSE Algorithms

Dr. Majid S. Naghmash, Reem Jamal Abbas, Rawaa AbdelRidha Kadhim

***Abstract*— In this research, the low noise portable wireless modem for patient ECG signal transfer based SDR technology is investigated and developed. The electrocardiogram (ECG) signal is obtained from human heart and sent to a personal watch fixed in the doctor hand to serve the emergency situation. The ECG signal is amplified and filtered using digital modem connected with either GSM or any other communication system like WLAN and mobile phone technology. Software Defined Radio (SDR) technology offers the reconfiguration and flexibility to eliminate the noise and interference from ECG signal in the receiver side. To overcome the noise problems associated with the ECG signals, the Fractional Space Equalizer (FSE) algorithms is used in the receiver side with accurate filtering in the baseband signals. In this techniques, the real time remotely checking is realized and the people could be monitored from outside of hospital and early treatment is promising. The proposed system enhance the human daily life and keep it more relaxed. Results shows the reality of the modem with low noise and interference.**

***Index Terms*— Wireless Modem, ECG,FSE, SDR**

I. INTRODUCTION

The most important problems in the healthcare is the electrocardiogram (ECG) signal which will stopped the human life instantaneously. In near future, the people over 70 years will become more than 700 million in the world which is twice of the 1990 rate[1]. However, healthcare providers are planning to develop a high quality and low cost systems to make people life more comfortable who suffer from heart diseases. Nowadays, the advance wireless communication systems becomes active research area to support and serve the requirements of consumer. Hence, the development of portable remote healthy monitoring systems enable observing of some diseases from hospitals. The objectives of healthcare development is to check and monitoring online medical parameters in order to reach this information from everywhere and anytime[2]. The implantation of this systems becomes more easy due to rapid growth in the communication technology. Additionally, the communication channel systems is mostly effected by noise and interference with excess medium and channels as well as delay spread introduced by inter symbol interference. Therefore, the transmission channel equalization should be used in this type of modem to compensate the unwanted outcome in the channel. To attain this objective, the equalizer uses an estimate of the channel frequency response, thought the fading channel vary all through the broadcast phase. The equalizer required here to study the frequency response in an adaptive style to be talented to incessantly alleviate the unenthusiastic outcome in the channel[3]. The obtainable equalization channels techniques like FSE with other types shows better performance [4]. Inter symbol Interference (ISI) is a form of distortion in which one symbol interferes with subsequent symbols. The ISI is an unwanted occurrence as the preceding symbols has alike effects as noise , hence making the communication fewer dependable. The multipath propagation is almost caused the ISI in the channel and the inherent non-linear frequency response produce successive symbols [5]. Many researcher is proposed their design in this field but with some limitation due to never used the SDR technology which offers good flexibility and re-programmability in the remote control technology. Additionally, the distance limitation is breakdown the designer objectives due to ECG frequency which is below 5-30 Hz. To enhance the capability of telemedicine, the ECG transmission via communication channels is developed and reported using LabView by [6] and [7]. In order to transmit the ECG signal, it is possible to digitalized first and convert the signal to packets [8]. The transmission of real time ECG signal through voice channel with minimum cost using GSM network has been introduced by [9]. The Zigbee technology and Bluetooth is used to transmit the biomedical data has been proposed by [10] and [11] respectively. In addition, the wireless sensor nodes is used to transfer the ECG signal from human heart to the monitoring staff by [12]. In this research, the ECG signal will process and transmitted to the doctor in charge using the most flexible and reconfigured technology represented by SDR idea. The SDR transceiver showing in Figure 1 has been modeled and developed to enhance the fast and easy healthcare using MATLAB and System Generator. The objective of this research is to transmit the biomedical data such as ECG signal from remot patient location to the

Manuscript received Feb. 26, 2014.

Dr. Majid S. Naghmash, Electrical Power Engineering Techniques, Fundation of Technical Education/ College of Electrical & Electronic Engineering Techniques / Ministry of high Education and scientific Research/Baghdad/ Iraq, /+9647812326878.

Reem Jamal Abbas, Computer Engineering Techniques, Foundation of Technical Education/College of Electrical & Electronic Engineering Techniques/ Ministry of high Education and scientific Research/ Baghdad/Iraq,/+9647901208744.

Rawaa AbdelRidha Kadhim, Computer Engineering Techniques, Foundation of Technical Education/ College of Electrical & Electronic Engineering Techniques/ Ministry of high Education and scientific Research/Baghdad/Iraq,/+9647713776664.

healthycare staff using the public GSM mobile phone in order to facilitate and rapidly treatment the emergency case. The smoothing of electrocardiogram (ECG) signal with noise and after equalizer fiter could be simulated using MATLAB as ullistrated in Figure 2. The noise level could be controlled by using FIR filter with different step size and vary filter order. The number of samples with frame size will indicate the performance of the ECG smooth degree. However, The ideal ECG signal is shown in the bottom of the figure for comparision reason.

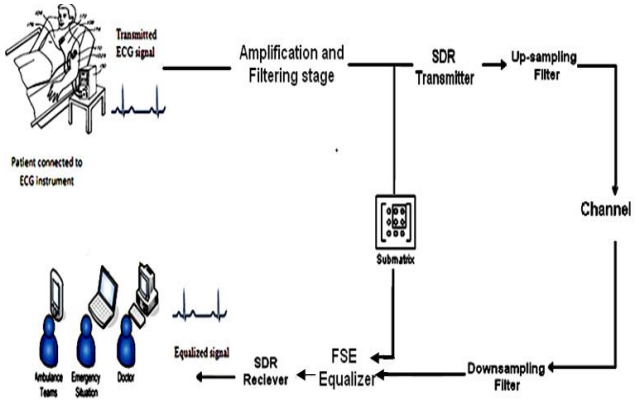

Figure 1: proposed ECG signal Transfare system

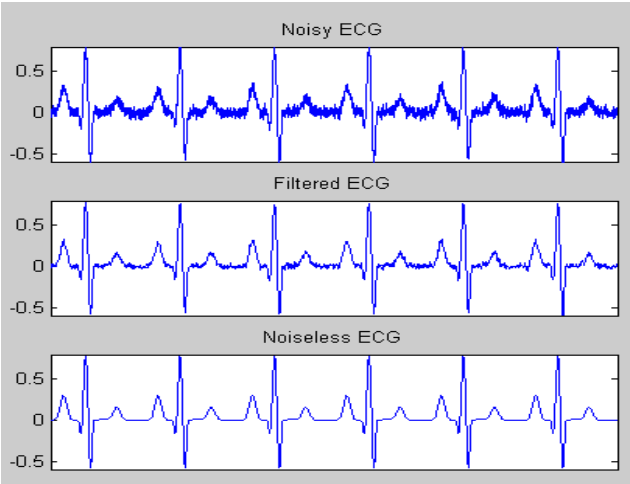

Figure 2: ECG signal with and without noise

The M-file code programs could be used to creat the ECG sinal in MATLAB assuming 89 beats per minuts and the peak amplitude voltage of 3.5 mv as shown in Figure 3.

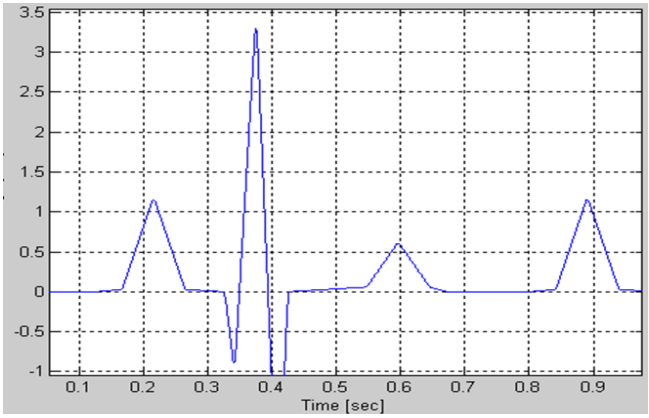

Figure 3: ECG signal specification

II. SDR Transceiver Design

The ECG signal is an electrical activity of human heart with 0.05-10 mV peak amplitude which need an amplified stage before send to SDR transciever. The power electricity line will generate 50 Hz noise and interference as well as other noise source like human body, passive circuit component, passive LPF and RC high pass filter. However, an operational amplifier must be used to amplify the ECG signal as first stage before sending to SDR transmitter. The FSE linear equalizer operating on QAM data source with noise and filtering introduced in the channel model. The FSE equalizer operate based on FSE algorithms with 64-taps filter. The standards constellation and eyes diagrams in MATLAB simulation model is used to test the transmit and receive signals. To minimize the error, the FSE algorithms is used in the receiver side after the transmit signal is contaminated by noise and ISI. The simulation can be broken down into three main stages, transmitter, channel and receiver. The modulation and demodulation steps are comprised of several distinct systems. The 16-QAM baseband signal is generated and passed through a channel. When the baseband signals are transmitted over a communication channel then they are distorted by various channel imperfections. The MATLAB model for proposed FSE equalizer has been developed as shown in Figure 4. In the receiver side, the incoming signals is mixed with noise and down converted into intermediate frequency and fined gain filtered signal is then pass through the FSE equalizer to be compared with transmitted signal then demodulated to recovered the original data. The modulated 16-QAM signal is passed through non linear IIR filter to generate ISI noise in the transmitter path.

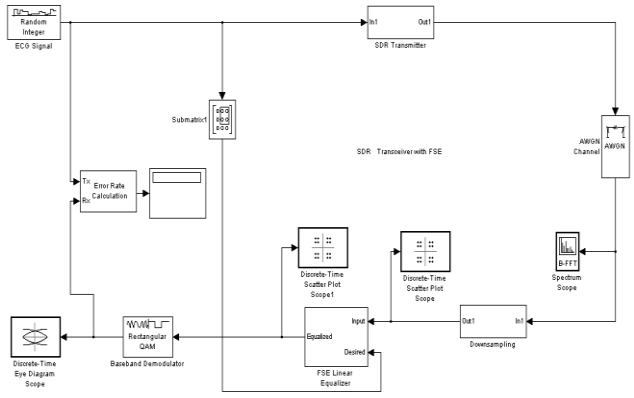

Figure 4: MATLAB SDR design with FSE algorithms

The transmitted signal is up converted and shaped by root raised cosine filter. After the transmitted signal is up converted it may lose some of properties, therefore the gain stage should be used to balance this loses before transmitted to the channel stage. The transmitter design model in MATLAB is illustrated in Figure 5.

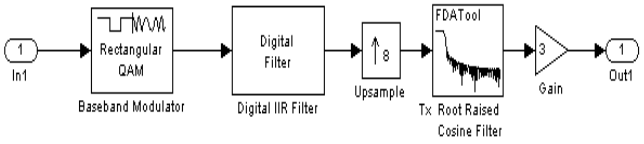

Figure 5: SDR transmitter link modeling

In the receiver path, the incoming signal with ISI and noise is down sampled and filtered by using root raise cosine filter and fine gain before equalize stage. The contaminated incoming signal is then passed through the FSE equalizer to remove all type of noise and ISI introduced by AWGN channel and non linear IIR filter respectively. Finally, the clean signal is demodulated and recovered to get the original data. The receiver link modeling is illustrated in Figure 6.

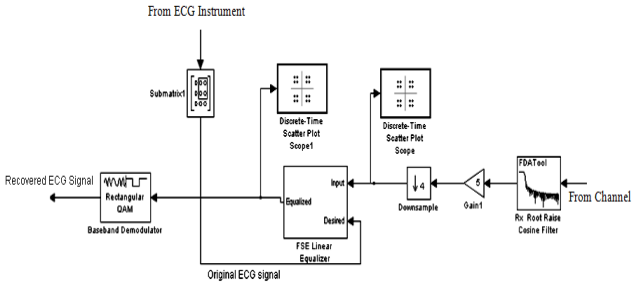

Figure 6: Receivers link modeling

The simulation results for 16-QAM scheme using FSE linear equalizer and conventional one. The constellation diagram for the transmitted signal is shown if Figure 7. Obviously, the signal is free from ISI before IIR filter. After the transmitted signal is passed through the non linear IIR filter, it's clearly suffered from ISI distortion introduced by the IIR Filter as shown in Figure 8.

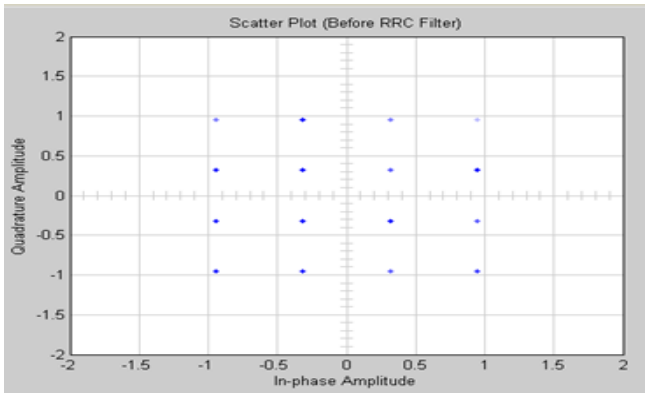

Figure 7: Constellation diagram of 16-QAM signal before IIR filter

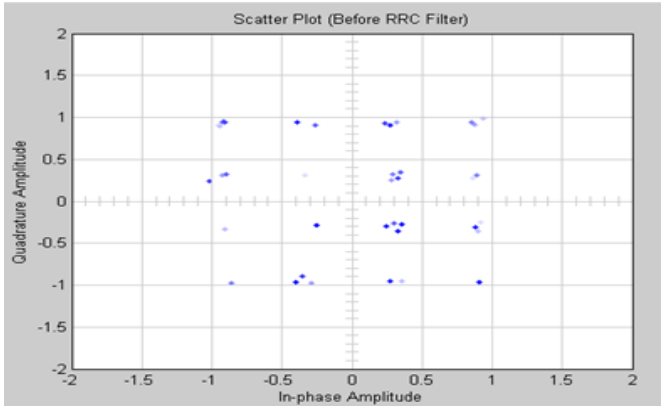

Figure 8: Constellation diagram of 16-QAM signal after IIR filter

Winning the receiver of the signal, the demodulator examine the received symbol, which may have been corrupted by the channel or the receiver noise (AWGN). As its estimated of what was actually transmitted, that point on the constellation diagram which is closed to that of the received symbol. However, it will demodulate incorrectly if the corruption has caused the received symbol to move closer to another constellation point than the transmitted one. In this case, the equalizer will play the main role to guide the received signal and eliminate the ISI and noise from the channel. The FSE Equalizer block uses a linear equalizer and the FSE algorithm to equalize a linearly modulated baseband signal through a dispersive channel. During the simulation, the block uses the FSE algorithm to update the weights, once per symbol. If the Number of samples per symbol parameter is 1, then the block implements a symbol-spaced equalizer; otherwise, the block implements a fractionally spaced equalizer.

The FSE Filter block can implement an adaptive FIR filter using five different algorithms. The block estimates the filter weights, or coefficients, needed to minimize the error between the output signal and the desired signal. This input signal can be a sample-based scalar or a single-channel frame-based signal. Connect the desired signal to the desired port. The desired signal must have the same data type, frame status, complexity, and dimensions as the input signal. The Output port outputs the filtered input signal, which is the estimate of the desired signal. The output of the Output port has the same frame status as the input signal. The Error port outputs the result of subtracting the output signal from the desired signal. However, the desired signal is connected to the transmit signal before IIR filter. The equalizer will compare between the transmitted symbol and the received one to correlate the correct symbol and feed to the demodulator. This block accepts only frame-based signals. If the value of Reference tap is equal to or greater than the frame size, the block will not work properly. The eye diagram of the received signal before and after the equalizer is shown in Figure 5. If one makes a look at the received signal, the signal is affected by ISI and noise effect with SNR of less than 20 dB. When the SNR increased to 30 dB, the noise margin start to close out and the error is decreased in eye diagram. Since, the SNR decrease to 10 dB, the eye diagram has more distortion in the system. Figure 6 shows the eye diagrams of the receiver signal when SNR = 30 dB. The eye diagram reveals less distortion given that the eye opening is more defined. The correct eye results and less bit error and hence, less transmission error. The received IQ signals are filtered and fine-gained to convert them into refined IQ signals. During the simulation, the block uses the FSE algorithm to update the weights, once per symbol. If the Number of samples per symbol parameter is 1, then the block implements a symbol-spaced equalizer; otherwise, the block implements a fractionally spaced equalizer.

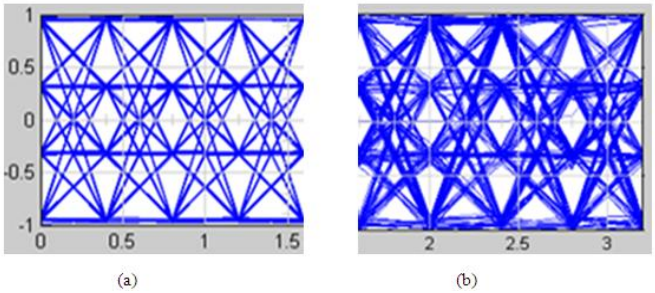

Figure 9: Eye diagram of 16-QAM received signal (a): after Equalizer, (b):before Equalizer

III. System Generator Design

The System Generator from Xilinx has been used to implement 64 filter taps with transmitter and receiver paths using 16-QAM modulation and demodulation scheme. The MAC FIR filter from Xilinx is also used here to reduce the multiplication process in the filter performance and to optimize the FPGA speed and resources. The Vertix-4 FPGA with Integrated Software Environment (ISE) software is used to synthesis the Hardware Description Language (HDL) code depend on Xilinx Synthesis Technology (XST) tool. After the adjustment of all FPGA constraint time which meet the chip requirements. The accurate synchronization between transmitter and receiver depend on peak symbol, the bit stream of proposed model is downloaded to the FPGA board Via JTAG adaptation program without error. The model shown in Figure 10 represent the model implementation in system generator block sets. The MAC FIR filter from Xilinx which represent multiplier less filter is used to design the FSE filter as show in Figure 11.

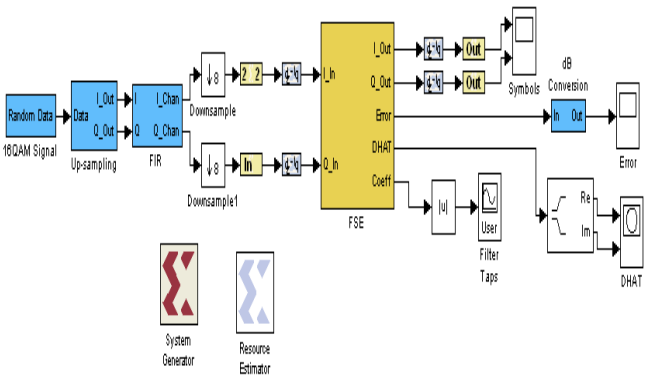

Figure 10: FSE implementation Using System Generator

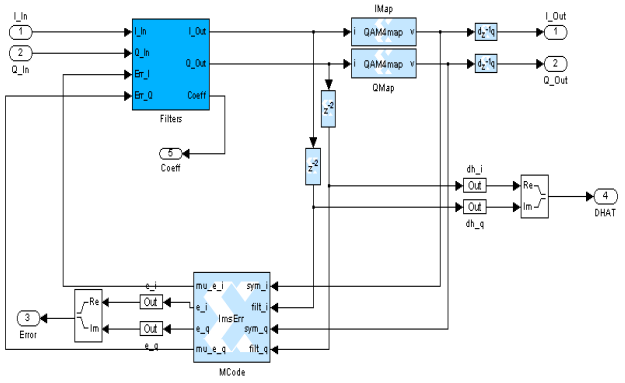

Figure 11: MAC FIR design using MCode

The ISE software generate the occupied Slices and LUTs utilization summery as illustrated in Table 1. The conventional design compared with proposed model consume more power due to large number of resources used as show in the comparison Table.

Table 1: Device Utilization Summary

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	1,159	30,720	3%	
Number of 4 input LUTs	980	30,720	3%	
Logic Distribution				
Number of occupied Slices	353	15,360	2%	
Number of Slices containing only related logic	334	353	94%	
Number of Slices containing unrelated logic	19	353	5%	
Total Number of 4 input LUTs	436	30,720	1%	
Number used as logic	295			
Number used as a route-thru	11			
Number used as Shift registers	130			
Number of bonded IOBs	61	448	13%	
Number of BUFG/BUFGCTRLs	4	32	12%	
Number used as BUFGs	4			
Number used as BUFGCTRLs	0			
Number of FIFO16/RAMB16s	8	192	4%	
Number used as FIFO16s	0			
Number used as RAMB16s	8			
Number of DSP48s	12	192	6%	
Total equivalent gate count for design	539,143			
Additional JTAG gate count for IOBs	2,928			

Table 2: Resource Comparison with Conventional design

Resource	G. Malik and A. Singh 2011	K. Veer et al. 2012	Proposed Model 2014	Improvements %
Slices	2232	2163	1159	46%
LUTs	1070	1251	980	21%

IV. Conclusion

A novel ECG signal transmission via GSM mobile network based SDR transceiver is developed and proposed with low ISI and channel noise. The efficient FSE equalizer is used in the receiver path to optimize the distortion generated in the channel which perform better performance than the conventional equalizer. Software based simulation approach has made easily to change system parameters, debug and test easy. The capability of proposed equalizer within SDR transceivers shows unlimited accuracy to recover the received symbol exactly like transmitted symbol and no error appear were the different between the transmit and received symbol is zero. The implementation results shows low power consumption in term of Slices and LUTs through FPGA resources. This development appear promising to support the current and future healthcare performance to overcome the problems in the conventional services.

References

[1] Kanwar Veer Partap, et al. 2012, "Performance Analysis Of Fractionally Spaced Adaptive Equalizer using 16QAM Receiver, International Journal of Engineering Research & Technology (IJERT) Vol. 1 Issue 6, pp. 1-4, August – 2012

[2] G. Malik, A. S. Sappal, "Fractionally Spaced Adaptive Equalizer for a 16-QAM Receiver", IJECT Vol. 2, Issue 3, pp. 61-64, Sept. 2011

[3] Guo Yecai; et al., "Design and Implementation of Adaptive Equalizer Based On FPGA" Electronic Measurement and Instruments, ICEMI '07. 8th International Conference Pp. 4-790-4-794, on Aug. 16- 2007

[4] Wei Zhang; Xiaoli Ma; Gestner, B.; Anderson, D.; "Designing low-complexity equalizers for wireless systems" Communications Magazine, IEEE Volume 47, Issue 1, Pp. 56 – 62.January 2009

[5] Amit Agarwal, "Design and Real Time Implementation of Adaptive Equalizer using Xilinx FPGA". Thesis, IIT Kharagpur, 2009.

[6] Xuan-Thang Vu, Nguyen Anh Duc, Trinh Anh Vu, "16-QAM Transmitter and Receiver Design Based on FPGA",5th IEEE Symposium on Electronic design, test and application ,pp. 95-98, 2010.

[7] R. sukanesh, "GSM based ECG telemedicine alert system", International journal of Computer Science and Application Issue 2010

[8] tasneem Ibrahim Abdullah, "Transmission of real time Clinical Diagnostic signals over the GSM network", IEEE Student of Conference of Research and development, 2011

[9] Nabil Hamza, "International Conference On Communication, Computer And Power (Icccp'09)",Muscat, February 2009.

[10] kinging Wong, "Real-time Heart rate Variability Detection on Sensor node", , Department of Electrical and Electronic Engineering, Curtin University of technology ,Miri, Malasia, IEEE Sensors Applications Symposium New Orleans, LA, USA-February, 2009

Majid S. Naghmash, Received His Msc. degree in the satellite communication engineering from University of Technology Baghdad – Iraq-2004 and Doctor of philosophy in wireless and mobile system from University Science Malaysia (USM) Malaysia –Penang -2011. He is currently a head of power engineering department at College of Electrical Power Engineering Techniques-Foundation of technical Education, Ministry of high education and scientific research-Iraq. He has been a full-time lecturer in the Computer Department , Baghdad, Iraq, since March 2012. He also worked as senior researcher in the Iraqi Center of Development and Research since 1994.

Reem Jamal Abbas, Received Her B.sc. Degree in Electronic and Communications Engineering from Al-Nahrain University, Baghdad-Iraq 2005 And Msc. Degree in Electronic Engineering from Al-Nahrain University Baghdad-Iraq-2009. She is an assistant Lecturer in Computer Department at College of Electrical and Electronic Engineering Techniques-Foundation of Technical Education, Ministry of High Education and Scientific Research-Iraq.

Rawaa AbdelRidha Kadhim, Received Her B.sc. Degree in Medical Engineering from Al-Nahrain University, Baghdad-Iraq 2006 And M.sc. Degree in Medical Engineering from Al-Nahrain University Baghdad- Iraq-2009, She is an assistant Lecturer in Computer Department at College of Electronic & Electrical Engineering Techniques-Foundation of Technical Education, Ministry of High Education and Scientific research-Iraq.